(19) World Intellectual Property Organization

International Bureau



(43) International Publication Date 12 August 2004 (12.08.2004)

PCT

(10) International Publication Number WO 2004/068426 A1

(51) International Patent Classification7:

G07F 7/10

(21) International Application Number:

PCT/JP2004/000961

- (22) International Filing Date: 30 January 2004 (30.01.2004)
- (25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data: 2003-024167

31 January 2003 (31.01.2003) J

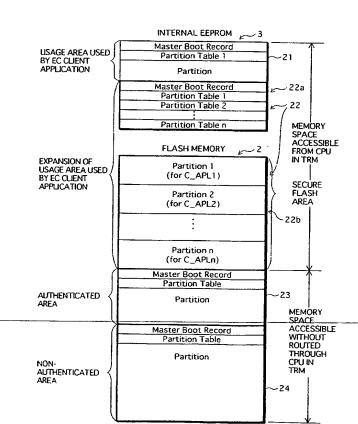
- (71) Applicant (for all designated States except US): MAT-SUSHITA ELECTRIC INDUSTRIAL CO., LTD. [JP/JP]; 1006, Oazakadoma, Kadoma-shi, Osaka 571-8501 (JP).
- (72). Inventors; and

(75) Inventors/Applicants (for US only): EBARA, Hiromi [/]. KAWANO, Shinji [/]. NAKABE, Futoshi [/].

- (74) Agent: NAKA,IMA, Shiro: 6F, Yodogawa 5-Bankan, 2-1, Toyosaki 3-chome, Kita-ku, Osaka-shi, Osaka 531-0072 (JP).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK,

[Continued on next page]

(54) Title: SEMICONDUCTOR MEMORY CARD, AND PROGRAM FOR CONTROLLING THE SAME



(57) Abstract: A semiconductor memory card that has a sufficient storage capaci ty when an electronic commerce (EC) application writes data to a storage is provided. A usage area for the EC application in an EEPROM 3 in a tamper resistant module (TRM) 1 is expanded. The expansion is such that a partition generated in a flash memory 2 outside the TRM 1 is assigned to the EC application while a partition table is allocated in the internal EEPROM 3. Because the partition table is in the TRM 1, only a CPU 7 in the TRM 1 is able to access the generated partition table. Secrecy of stored contents increases because the access to the expanded area is limited to the CPU 7 in the TRM 1.

BEST AVAILABLE COFT